Code.No: **RR311402** | RR | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL ELECTRONICS
(MECHANICAL ENGINEERING)
(MECHATRONICS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Explain the principle of operation of a clamper circuit.
b) What are the disadvantages of series and shunt clippers?
c) What is clamping circuit theorem? [16]

2.a) Derive the expression for period of oscillations of an Astable multivibrator circuit.
b) Design a collector coupled monostable multivibrator to produce a time delay of $80\,\mu$ Sec. Use transistor have h_{FE} of 150. Use $\pm$ 12 V source, V_{CE} Sat = 0.3V, V_{BE} sat = 0.7V, V_{BE} cutoff = 0.1V. [8+8]

3.a) Derive the expression for UTP and LTP in submit trigger by making necessary assumptions.
b) Explain the operation of current sweep circuit. List the applications of current sweep circuits. [8+8]

4.a) What are the self complementing codes and explain them with examples.
b) Implement the following functions using AND –OR-NOT gates
$f_1(A, B, C, D) = \Sigma\ (0, 2, 5, 6, 7, 8, 10)$
$f_2(A, B, C, D) = \Pi\ (1, 3, 5, 7, 11, 14)$. [8+8]

5.a) Design a full adder using MUX
b) Prove that NAND gate is an universal gate. [8+8]

6.a) Implement a JK flip flop using SR flip flops.
b) What are the excitations takes of D, T, JK and SR flip flops. [8+8]

7.a) Explain in detail a 4 bit up/ down counter with Timing diagrams.
b) What are the four different possible configurations of shift registers? Draw a general 4-bit shift register and its timing diagrams. [8+8]

8.a) Design a BCD to 7 segment decoder circuit.
b) Write a brief note on frequency synthesizer. [8+8]

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Code.No: **RR311402** | RR | SET-2

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL ELECTRONICS
(MECHANICAL ENGINEERING)
(MECHATRONICS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1.a) Derive the expression for UTP and LTP in submit trigger by making necessary assumptions.
b) Explain the operation of current sweep circuit. List the applications of current sweep circuits. [8+8]

2.a) What are the self complementing codes and explain them with examples.
b) Implement the following functions using AND –OR-NOT gates
$f_1(A, B, C, D) = \Sigma\ (0, 2, 5, 6, 7, 8, 10)$
$f_2(A, B, C, D) = \Pi\ (1, 3, 5, 7, 11, 14)$. [8+8]

3.a) Design a full adder using MUX
b) Prove that NAND gate is an universal gate. [8+8]

4.a) Implement a JK flip flop using SR flip flops.
b) What are the excitations takes of D, T, JK and SR flip flops. [8+8]

5.a) Explain in detail a 4 bit up/ down counter with Timing diagrams.
b) What are the four different possible configurations of shift registers? Draw a general 4-bit shift register and its timing diagrams. [8+8]

6.a) Design a BCD to 7 segment decoder circuit.
b) Write a brief note on frequency synthesizer. [8+8]

7.a) Explain the principle of operation of a clamper circuit.
b) What are the disadvantages of series and shunt clippers?
c) What is clamping circuit theorem? [16]

8.a) Derive the expression for period of oscillations of an Astable multivibrator circuit.
b) Design a collector coupled monostable multivibrator to produce a time delay of $80\,\mu$ Sec. Use transistor have h_{FE} of 150. Use $\pm$ 12 V source, V_{CE} Sat = 0.3V, V_{BE} sat = 0.7V, V_{BE} cutoff = 0.1V. [8+8]

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Code.No: **RR311402** | RR | SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL ELECTRONICS
(MECHANICAL ENGINEERING)
(MECHATRONICS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1.a) Design a full adder using MUX
b) Prove that NAND gate is an universal gate. [8+8]

2.a) Implement a JK flip flop using SR flip flops.
b) What are the excitations takes of D, T, JK and SR flip flops. [8+8]

3.a) Explain in detail a 4 bit up/ down counter with Timing diagrams.
b) What are the four different possible configurations of shift registers? Draw a general 4-bit shift register and its timing diagrams. [8+8]

4.a) Design a BCD to 7 segment decoder circuit.
b) Write a brief note on frequency synthesizer. [8+8]

5.a) Explain the principle of operation of a clamper circuit.
b) What are the disadvantages of series and shunt clippers?
c) What is clamping circuit theorem? [16]

6.a) Derive the expression for period of oscillations of an Astable multivibrator circuit.
b) Design a collector coupled monostable multivibrator to produce a time delay of $80\,\mu$ Sec. Use transistor have h_{FE} of 150. Use $\pm$ 12 V source, V_{CE} Sat = 0.3V, V_{BE} sat = 0.7V, V_{BE} cutoff = 0.1V. [8+8]

7.a) Derive the expression for UTP and LTP in submit trigger by making necessary assumptions.
b) Explain the operation of current sweep circuit. List the applications of current sweep circuits. [8+8]

8.a) What are the self complementing codes and explain them with examples.
b) Implement the following functions using AND –OR-NOT gates
$f_1(A, B, C, D) = \Sigma\ (0, 2, 5, 6, 7, 8, 10)$
$f_2(A, B, C, D) = \Pi\ (1, 3, 5, 7, 11, 14)$. [8+8]

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Code.No: **RR311402** | RR | SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL ELECTRONICS
(MECHANICAL ENGINEERING)
(MECHATRONICS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Explain in detail a 4 bit up/ down counter with Timing diagrams.
b) What are the four different possible configurations of shift registers? Draw a general 4-bit shift register and its timing diagrams. [8+8]

2.a) Design a BCD to 7 segment decoder circuit.
b) Write a brief note on frequency synthesizer. [8+8]

3.a) Explain the principle of operation of a clamper circuit.
b) What are the disadvantages of series and shunt clippers?
c) What is clamping circuit theorem? [16]

4.a) Derive the expression for period of oscillations of an Astable multivibrator circuit.
b) Design a collector coupled monostable multivibrator to produce a time delay of $80\,\mu$ Sec. Use transistor have h_{FE} of 150. Use $\pm$ 12 V source, V_{CE} Sat = 0.3V, V_{BE} sat = 0.7V, V_{BE} cutoff = 0.1V. [8+8]

5.a) Derive the expression for UTP and LTP in submit trigger by making necessary assumptions.
b) Explain the operation of current sweep circuit. List the applications of current sweep circuits. [8+8]

6.a) What are the self complementing codes and explain them with examples.
b) Implement the following functions using AND –OR-NOT gates
$f_1(A, B, C, D) = \Sigma\ (0, 2, 5, 6, 7, 8, 10)$
$f_2(A, B, C, D) = \Pi\ (1, 3, 5, 7, 11, 14)$. [8+8]

7.a) Design a full adder using MUX
b) Prove that NAND gate is an universal gate. [8+8]

8.a) Implement a JK flip flop using SR flip flops.
b) What are the excitations takes of D, T, JK and SR flip flops. [8+8]

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